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(54) Low drop-out voltage regulator

(57) A low drop-out voltage regulator having a pass device (M_P), an error amplifier (M_1-M_{51}) and a double regulation loop including DC feedback loop (R_1, R_2) and an AC feedback loop (R_F, C_F) including a high pass filter (C_F). Combining these two loops creates an ultra low frequency internal pole which makes the regulator stable substantially independent of the output bypass capacitor's value.
This provides the following advantages: allows the use of very low bypass capacitors; allows to extend the PSRR frequency behavior; allows an increase in the regulator's efficiency (reduced power consumption on heavy loads).

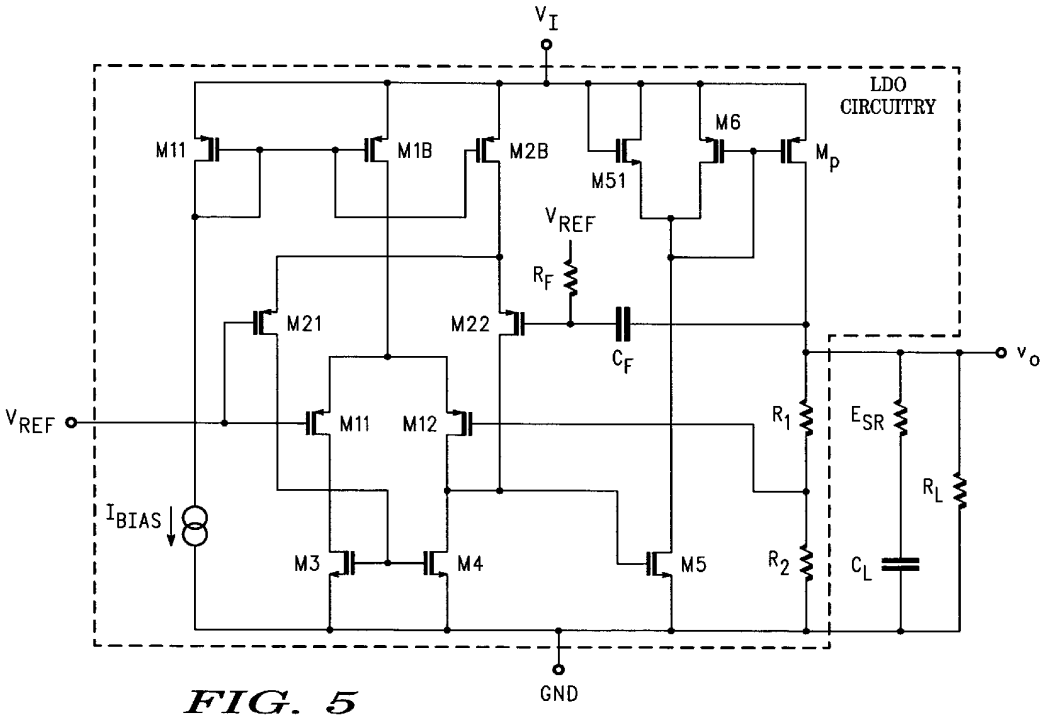

FIG. 5

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Description

Field of the Invention

[0001] This invention relates to voltage regulators, and particularly to low drop-out (LDO) voltage regulators.

Background of the Invention

[0002] A low drop-out voltage regulator is a regulator circuit that provides a well-specified and stable DC voltage (whose input-to-output voltage difference is typically low). The operation of the circuit is based on feeding back an amplified error signal which is used to control output current flow of a pass device (such as a power transistor) driving a load. The drop-out voltage is the value of the input/output differential voltage where regulation is lost.

[0003] The low drop-out nature of the regulator makes it appropriate (over other types of regulators such as dc-dc converters and switching regulators) for use in many applications such as automotive, portable, and industrial applications. In the automotive industry, the low drop-out voltage is necessary during cold-crank conditions where an automobile's battery voltage can be below 6V. Increasing demand for LDO voltage regulators is also apparent in mobile battery operated products (such as cellular phones, pagers, camera recorders and laptop computers), where the LDO voltage regulator typically needs to regulate under low voltage conditions with a reduced voltage drop.

[0004] A typical, known LDO voltage regulator uses a differential transistor pair, an intermediate stage transistor, and a pass device coupled to a large (external) bypass capacitor. These elements constitute a DC regulation loop which provides voltage regulation.

[0005] Depending on the application, a critical component of the regulator is often its bypass capacitor. Indeed, to ensure stability under all operating conditions, large values of capacitor are used. This translates into large area on the PCB on which the regulator circuit is built, and higher costs.

[0006] However, this known LDO voltage regulator has the disadvantages that it is difficult (i) to significantly reduce the bypass capacitor below approximately 1μF per 10mA output current capability, and (ii) to significantly increase the PSRR frequency behavior without high increase of power consumption.

[0007] A need therefore exists for a low drop-out voltage regulator wherein the abovementioned disadvantage(s) may be alleviated.

Statement of Invention

[0008] In accordance with the present invention there is provided low drop-out voltage regulator as claimed in claim 1.

[0009] At least in a preferred form, the present invention allows the use of capacitors lower than 1μF overall, allowing costs to be significantly reduced, and ensures good stability (even if no external output capacitor is used - providing the most cost-efficient solution for applications where the transient response of the regulator is not a critical requirement). Also, since low capacitors have low serial resistance, the design of the LDO is made easier. In a preferred form the invention achieves such performance without increasing the overall power consumption of the LDO voltage regulator.

Brief Description of the Drawings

[0010] One low drop-out regulator incorporating the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

FIG. 1 shows a block-schematic circuit diagram of a typical, classical low drop-out voltage regulator;

FIG. 2 shows a block-schematic circuit diagram of a simplified practical implementation of the LDO voltage regulator of FIG. 1;

FIG. 3 shows a block-schematic circuit diagram illustrating the open-loop AC-model of the LDO voltage regulator of FIG. 2;

FIG. 4 shows a graphical illustration of the stability of the LDO voltage regulator of FIG. 2 under conditions of varying load;

FIG. 5 shows a block-schematic circuit diagram of an LDO voltage regulator incorporating the present invention;

FIG. 6 shows a block-schematic circuit diagram illustrating the open-loop AC model of the LDO voltage regulator of FIG. 5; and

FIG. 7 shows a graphical illustration, similar to FIG. 4, of the open-loop performance of the LDO voltage regulator of FIG. 5.

Description of Preferred Embodiment(s)

[0011] A classic, known low drop-out regulator is depicted in FIG. 1. It is partitioned into 3 main parts : Pass-device (MOS transistor M_p - having transconductance $G_M(p)$ and resistance R_{dsp}), error amplifier ($A(p)$) and resistor feedback (R_1,R_2). The pass-device M_p is used as a current-source, which is driven by the error amplifier ($A(p)$) to pass a current I_I from an input voltage V_I. The output voltage V_O is divided by the resistor ladder R_1, R_2 and compared with reference voltage V_{REF}. The current in the pass-device M_p is controlled according to this difference. Bypass capacitor C_L (having electrical series resistance E_{SR}) is connected to the the output, and output resistance of the load is represented by R_L. The output voltage is given by :

$$V_O = V_{REF}\left(1+\frac{R_1}{R_2}\right) \qquad (1)$$

To obtain a low drop-out voltage, a PMOS pass device is the most convenient transistor for power management applications.

[0012] Most low-dropout regulators designs use the regulation architecture combined with pole-tracking. Even if topologies are changing to improve a given specification requirement, pole tracking is a common and an efficient design technique. Indeed, to prevent instability due to changes of the output current, a local feedback is used to perform a tracking between the output pole and the pole of the intermediate stage. FIG. 2 shows a simplified schematic of a practical implementation of the LDO voltage regulator of FIG. 1, typically used for wireless applications. In the circuit of FIG. 2, the differential pairs of MOS transistors M_1-M_4 constitute the first stage of the amplifier and drive an intermediate stage M_5,M_6,M_{51}. The amplifier has an input stage constituted by MOS transistors M_{11} and M_{12} producing a current I_T, and is biased by a current source producing a bias current I_{BIAS}.

[0013] Pole-tracking is implemented using the current mirror between M_P and M_6. By feeding a part of the current of the pass-device in the intermediate stage, the impedance and the pole of this stage tracks the output impedance/pole. However, although it is easier to stabilize the regulator of FIG. 2 under variations in load current I_{LOAD} using the pole tracking scheme, the inventors of the present invention have recognized that the problem of stability regarding variations of E_{SR} is still unsolved since there is no means to sense the value of this serial resistance.

[0014] The absolute stability of a regulator is an implicit specification, which is the root cause of many trade-offs in designing the regulator. Before considering the stability of the regulator in more detail, its open-loop frequency response must be calculated.

[0015] FIG. 3 shows the AC model of the low drop-out regulator of FIG. 2. In the model of FIG. 3, the low drop-out regulator of FIG. 2 is modeled as follows:

- the differential stage (transistors M_1-M_4) is modeled by an amplifier of gain $-g_{m1}$, a resistor R_{o1} and a capacitor C_{o1};
- the intermediate stage (transistors M_5,M_6,M_{51}) is modeled by an amplifier of gain $-g_{m2}$, a resistor R_{o2} and a capacitor C_{gs};
- the pass device M_p is modeled by the capacitor C_{gs}, a voltage controlled current source driven by a voltage V_{gs} and a resistor R_{dsp};
- the load section is modeled by the resistor E_{SR} and capacitor C_L and the resistor R_L; and
- the feedback loop is modeled by the resistors R_1 and R_2.

[0016] The open-loop gain of this model is:

$$\text{OpenLoopGain}(s) = \frac{N_{OLG}(s)}{D_{OLG}(s)} \qquad (2)$$

where $N_{OLG}(s) = -R_2 g_{m1} r_{o1} g_{m2} r_{o2} g_{mp} R_s (1+E_{SR}C_L s)$
$D_{OLG}(s)=(R_1+R_2)(1+R_{o1}C_{o1}s)(1+R_{o2}C_{gs}s)(1+(E_{SR}+R_S)C_L s)$ and

$R_S=(R_1+R_2)//R_L//R_{dsp}$, '//' indicating 'in parallel'.

[0017] The open-loop DC gain of the model is:

$$A_{OL}(DC)=\frac{R_2}{R_1+R_2}g_{m1}r_{o1}g_{m2}r_{o2}g_{mp}R_s \quad (3)$$

[0018] The system has 3 poles and 1 zero. The main pole is the pole of the output stage:

$$F_{OUT} = \frac{1}{2\pi(E_{SR}+R_S)C_L}$$

[0019] $\mathbf{E_{SR}}$ is low compared to $\mathbf{R_S}$ and can be neglected. It can be seen that this pole is a function of the load, which means that it changes with the load current. The relation is direct proportional and the pole frequency increases directly with the output current.
It should be noted that the low-frequency gain of the output stage is given by the equation :

$$A_{outputstage}(DC)=g_{mp}R_s \propto g_{mp}R_s$$

[0020] It is also a function of the output current, but the relation is different to that of the pole. $\mathbf{G_m}$ changes with the square root of the load current. $\mathbf{R_L}$, which represents the load current, varies directly with the current. This means that the gain decreases with the square root of the load current. Finally, when the output current increases, the output pole increases faster than the open-loop gain decreases. Depending on the design and the operating conditions, the pole of the differential stage is placed before or after that of the intermediate stage:

$$F_{pdiff} = \frac{1}{2\pi R_{o1}C_{o1}}$$

$$F_{pint} = \frac{1}{2\pi R_{o2}C_{gs}}$$

[0021] The zero is created by the $\mathbf{E_{SR}}$ of the output capacitor:

$$Z_{ESR} = \frac{1}{2\pi E_{SR}C_L}$$

[0022] It is obvious that such a system can be unstable under certain conditions. To simplify the study of the stability, the problem is split into 2 cases :

- $\mathbf{E_{SR}}$ is constant and the output current varies, and
- the output current is constant and $\mathbf{E_{SR}}$ varies.

[0023] $\mathbf{F_{pout}}$ is the main pole and varies with the output current. If $\mathbf{I_{LOAD}}$ is minimum $\mathbf{F_{pout}}$ is placed at low-frequencies. At the opposite extreme, when $\mathbf{I_{LOAD}}$ is maximum, $\mathbf{F_{pout}}$ is a high-frequency pole. FIG. 4 depicts the problem of stability, when the output current goes from its minimum to its maximum value (minimum value of the current in the pass-device is set by the feedback resistor). These curves show that if the system is stable under low-load conditions, it is not stable when the regulator operates under heavy-load conditions. Indeed, when changing from low to heavy load, the open-loop DC gain $\mathbf{A_{OL}}$ decreases proportionally with the square-root of the current in the pass-device, but the output pole is pushed toward high-frequencies proportionally to this current. This is why the frequency response crosses the 0 dB-axis with a slope of -40dB/decade leading to the instability of the system. This analysis explains the use of the pole-tracking scheme implemented in most of regulators.

[0024] The effect of the pole tracking is depicted in FIG. 4. By pushing $\mathbf{F_{pint}}$ toward high-frequencies proportionally to the output current, the 0 dB-axis is now crossed with a slope of -20 dB/decade.

[0025] It may be noted that since the zero due to E_{SR} and the poles of the differential pair and the intermediate stage are constant, the gain between the frequencies Z_{ESR} and F_{pdiff} is higher under heavy-load conditions than for low-load conditions, explaining why the stability is more critical under heavy-load operations.

[0026] Referring now to FIG. 5, a new, improved LDO voltage regulator adds an extra feedback loop to the classical architecture (e.g., FIG. 2). Compared with the prior art LDO of FIG. 2, the LDO of FIG. 5 includes additional MOS transistors M_{2B}, M_{21} and M_{22}, together with capacitor C_F (and resistor R_F through which reference voltage V_{REF} is applied). The LDO regulator circuit as shown in FIG. 5 is typically fabricated substantially entirely (the portion within the dashed line) in integrated circuit form, only the bypass capacitor and load (represented by the components E_{SR}, C_L and R_L) being external to the integrated circuit.

[0027] The LDO of FIG. 5 thus includes a feedback loop (as in the prior art LDO of FIG. 2) formed by R_1, R_2 and the differential pair M_{11}, M_{12}. Additionally, the LDO of FIG. 5 includes an extra feedback loop containing R_F, C_F and the second differential pair M_{21}, M_{22}. Due to the high-pass filter formed by R_F and C_F this additional feedback does not act at DC but in middle-frequencies; it helps to regulate the output voltage and to stabilize the system. A large value for R_F is implemented by using an integrated resistor or a depletion transistor with a large length.

[0028] As will be discussed in more detail below, Combining these two feedback loops creates an ultra low frequency internal pole which makes the regulator stable, substantially independent of the value (or, with particular applicability to applications where the transient response of the regulator is not a critical requirement, even the absence) of the output bypass capacitor. Also, since low capacitors have low serial resistance, the design of the LDO is made easier. Further, it will be understood that, thanks to the high pass filter provided by C_F, the extra feedback loop increases the PSRR for high frequencies.

[0029] The system of FIG. 5 has two loops which have to be opened and analyzed separately. Using a simplified AC-model such as depicted in FIG. 6, the poles and zeroes of the main loop can be found.

[0030] As shown in FIG. 6, the LDO of FIG. 5 is modeled as follows:

- the differential stages of transistors M_1-M_4, M_{21} & M_{22} and M_{11} & M_{12} are modeled by amplifiers of gain $-g_{m21}$ & $-g_{m11}$, a resistor R_{o1} and a capacitor C_{o1};
- the intermediate stage (transistors M_5,M_6,M_{51}) is modeled by an amplifier of gain $-g_{m2}$, a resistor R_{o2} and a capacitor C_{gs};
- the pass device M_p is modeled by the capacitor C_{gs}, a voltage controlled current source driven by a voltage V_{gs} and a resistor R_{dsp};
- the load section is modeled by the resistor E_{SR} and capacitor C_L and the resistor R_L;
- the main feedback loop is modeled by the resistors R_1 and R_2; and
- the AC feedback loop is modeled by R_F and C_F.

[0031] The open-loop gain at DC for the main loop is :

$$A_{OL_{MAIN\text{-}LOOP}}(DC) = \frac{R_2}{R_1+R_2} g_{m11} r_{o1} g_{m2} r_{o2} g_{mp} R_s \qquad (4)$$

[0032] Equation (4) clearly shows that the DC performance of the LDO of FIG. 5 is not impacted by the extra feedback loop.

[0033] The main loop has now 2 zeroes instead of 1 in the classical configuration of FIG. 2, and 4 poles instead of 3. With this new structure, the first pole is now:

$$P_1 = \frac{1}{2\pi A_2 R_F C_F} \text{ with } A_2 = g_{m21} r_{o1} g_{m2} r_{o2} g_{mp} R_s$$

[0034] The low-frequency zero is created by the high-pass filter:

$$Z_2 = \frac{1}{2\pi R_F C_F}$$

[0035] It is followed by two (real or complex) poles P_2, P_3 related to the second order term:

$$1\text{-}Z_4 s + \frac{Z_4^2 T_2}{T_2\text{-}Z_4} s^2$$

[0036] The previous location of poles and zeroes clearly shows that the extra feedback loop creates a very low frequency pole which is internal while reducing the effect of the output stage on the regulator's stability. If $\mathbf{A_2}$ is large enough, the pole-tracking scheme is no longer required. Finally, the power consumption at full load is improved.

[0037] This very low-frequency pole related to the new LDO of FIG. 5 implies a very good phase margin of the system with high output currents and very low output capacitors. The locations of the new poles and zeroes are depicted FIG. 7, which shows the open-loop gain of the DC-feedback loop without (lower line) and with (upper line) a frequency-peak.

[0038] The stability of the extra feedback loop may be analysed from the following expression for the open-loop gain of the extra feedback loop:

$$A_{OL_{2nd-LOOP}}(s) = \frac{A_{OL_{MAIN-LOOP}}(DC)\cdot(R_F C_F s)\cdot(1+E_{SR}C_L s)}{(1+R_F C_F s)\cdot\left(1+\left(E_{SR}+\frac{R_F}{A_1}C_L s\right)R_F C_F s\right)\cdot\left(1+\left(\frac{R_S\cdot R_{o2}}{A_1 E_{SR}+R_S}\right)C_{gs}s\right)\cdot(1+R_{o1}C_{01})}$$

where

$$A_{OL_{2nd\text{-}LOOP}}(DC)=g_{m21}r_{o1}g_{m2}r_{o2}g_{mp}R_s$$

and

$$A_1 = \frac{R_2}{R_1+R_2}\, g_{m11}r_{o1}g_{m2}r_{o2}g_{mp}R_s$$

[0039] The locations of the poles and zeroes and the stability analysis can be deduced from the above equation for $\mathbf{A_{OL_{2nd\text{-}LOOP}}(s)}$.

[0040] It will be appreciated that, due to the capacitor C_F, the extra feedback loop provides only AC feedback. As previously explained, this loop acts at middle frequencies. Since the feedback voltage is directly taken at the output of the regulator, this new arrangement provides an increase in the bandwidth of the PSRR.

[0041] It will be understood that the improved low drop-out regulator described above provides the following advantages:

- Allows the use of very low bypass capacitors (which, with particular applicability to applications where the transient response of the regulator is not a critical requirement, may even be absent). Also, since low capacitors have low serial resistance, the design of the LDO is made easier.
- Allows extended bandwidth of PSRR frequency behavior.
- Allows increased regulator efficiency (reduced power consumption with heavy loads).

Claims

1. A low drop-out voltage regulator comprising:

   pass means **(M_P)** for controlledly passing a current from an input voltage applied thereto to produce a controlled output voltage;
   feedback means, including a DC feedback loop **(R_1, R_2),** for providing a feedback signal representative of the output voltage; and
   error amplifier means **(M_1-M_{51})** for comparing the feedback signal with a predetermined voltage and for producing a signal in dependence on the comparison for controlling the pass means;

   characterized in that:

the feedback means also includes an AC feedback loop (R_F, C_F), for operating in combination with the DC feedback loop.

2. The low drop-out voltage regulator of claim 1 wherein the AC feedback loop includes a high pass filter (C_F).

3. The low drop-out voltage regulator of claim 1 or 2 wherein the feedback voltage of the AC feedback loop is taken directly at the regulator's output.

4. The low drop-out voltage regulator of claim 1, 2 or 3 wherein the AC feedback loop includes a large value resistor (R_F) formed by an integrated resistor.

5. The low drop-out voltage regulator of claim 1, 2 or 3 wherein the AC feedback loop includes a large value resistor (R_F) formed by a depletion transistor with a large length.

6. An integrated circuit comprising a low drop-out voltage regulator of any preceding claim.

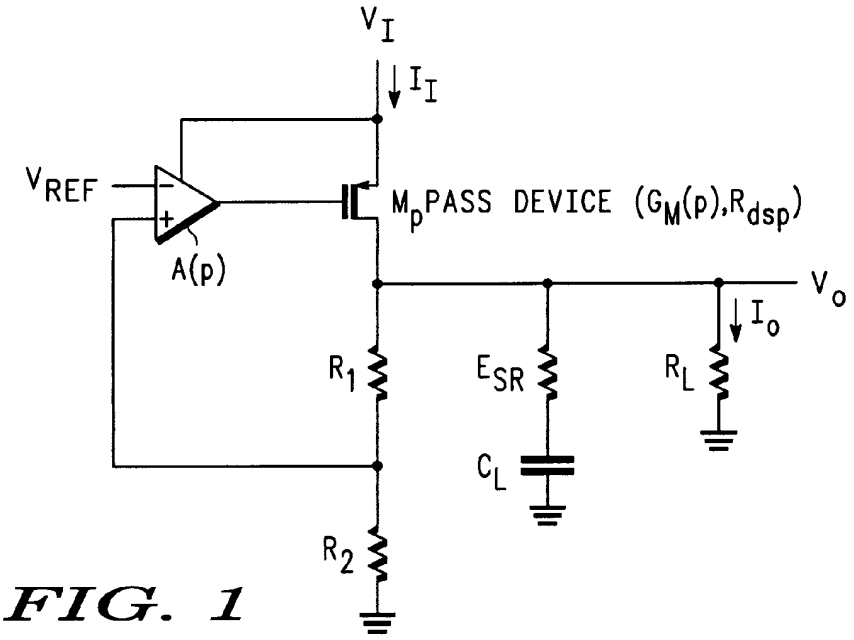


FIG. 1

-PRIOR ART-

FIG. 2

-PRIOR ART-

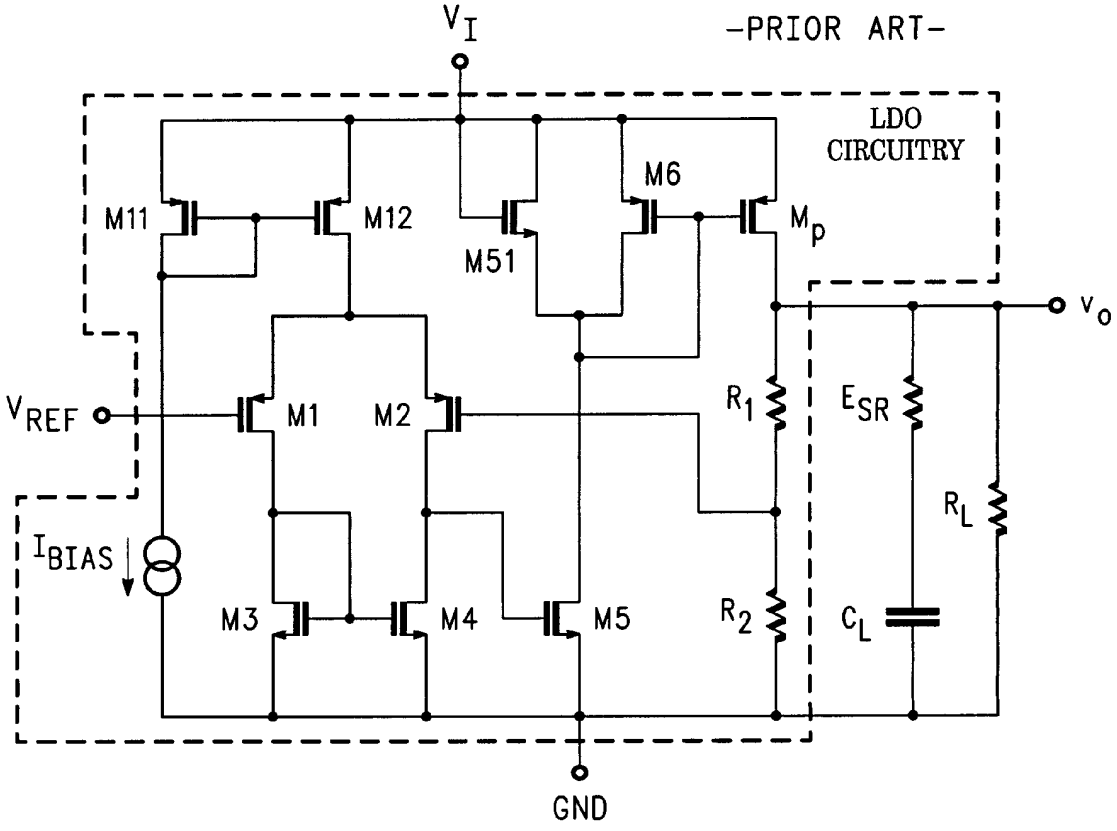
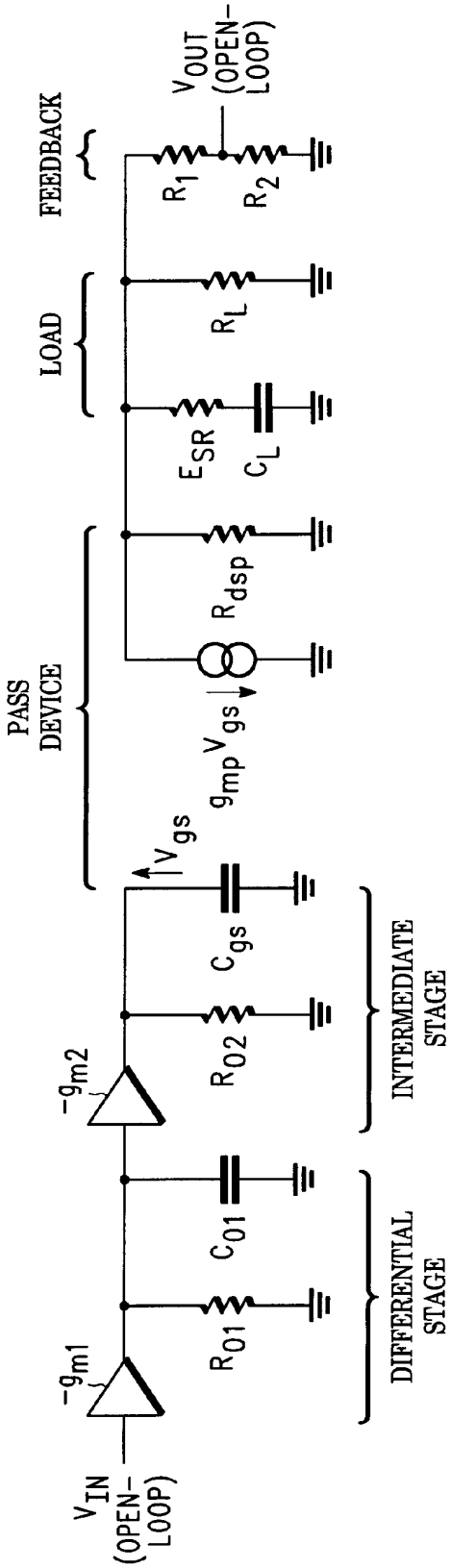


FIG. 3


V_IN (OPEN-LOOP)
-g_m1
R_O1
C_O1
-g_m2
R_O2
C_gs
V_gs
g_mp V_gs
R_dsp
E_SR
C_L
R_L
R_1
R_2
V_OUT (OPEN-LOOP)
DIFFERENTIAL STAGE
INTERMEDIATE STAGE
PASS DEVICE
LOAD
FEEDBACK

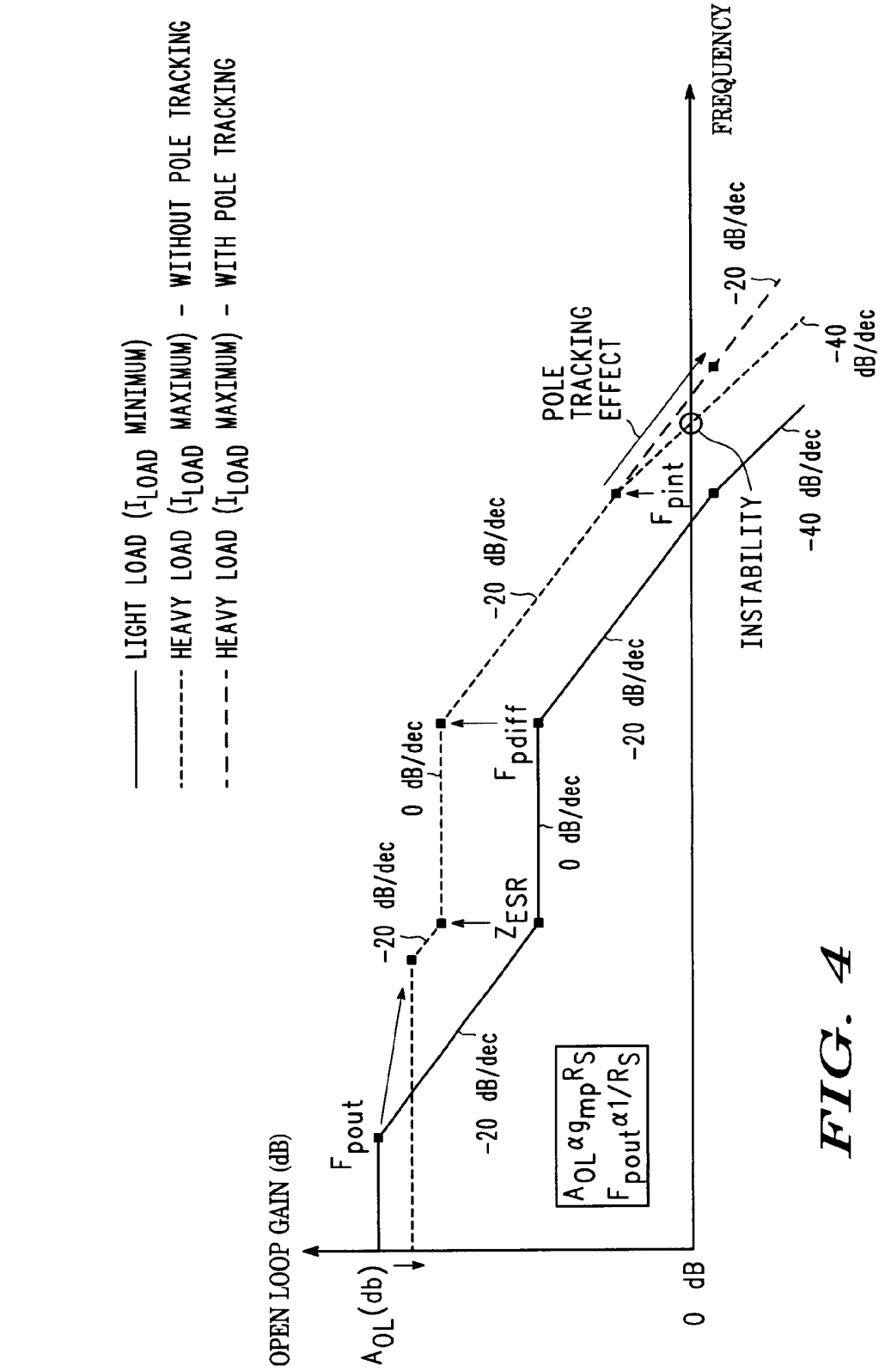

LIGHT LOAD (I_{LOAD} MINIMUM)
HEAVY LOAD (I_{LOAD} MAXIMUM) - WITHOUT POLE TRACKING
HEAVY LOAD (I_{LOAD} MAXIMUM) - WITH POLE TRACKING
OPEN LOOP GAIN (dB)
A_{OL}(db)
0 dB
FREQUENCY
F_{pout}
Z_{ESR}
F_{pdiff}
F_{pint}
-20 dB/dec
0 dB/dec
-20 dB/dec
-20 dB/dec
-20 dB/dec
-40 dB/dec
-40 dB/dec
POLE TRACKING EFFECT
INSTABILITY
$A_{OL} \alpha g_{mp} R_S$
$F_{pout} \alpha 1/R_S$

FIG. 4

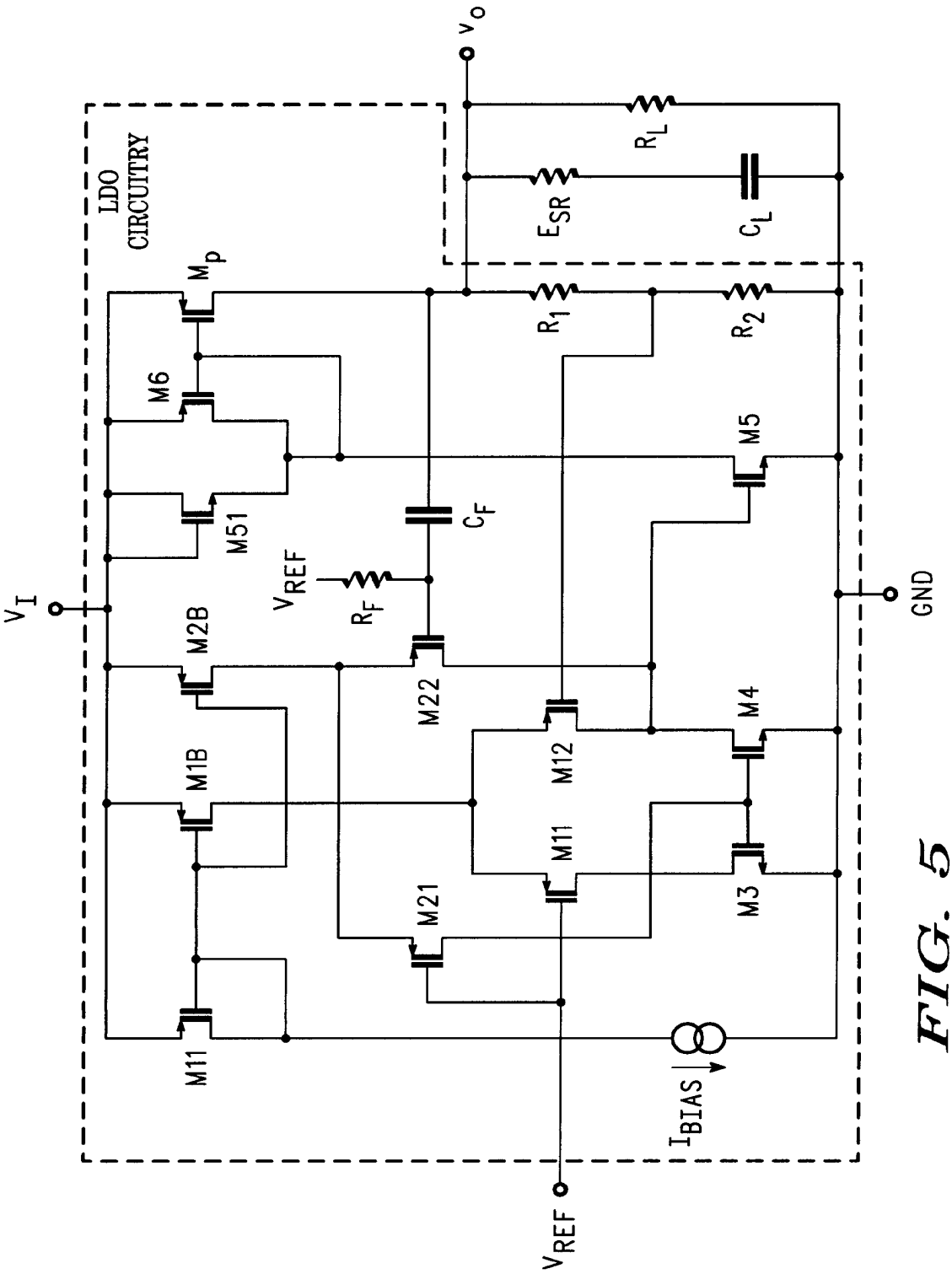
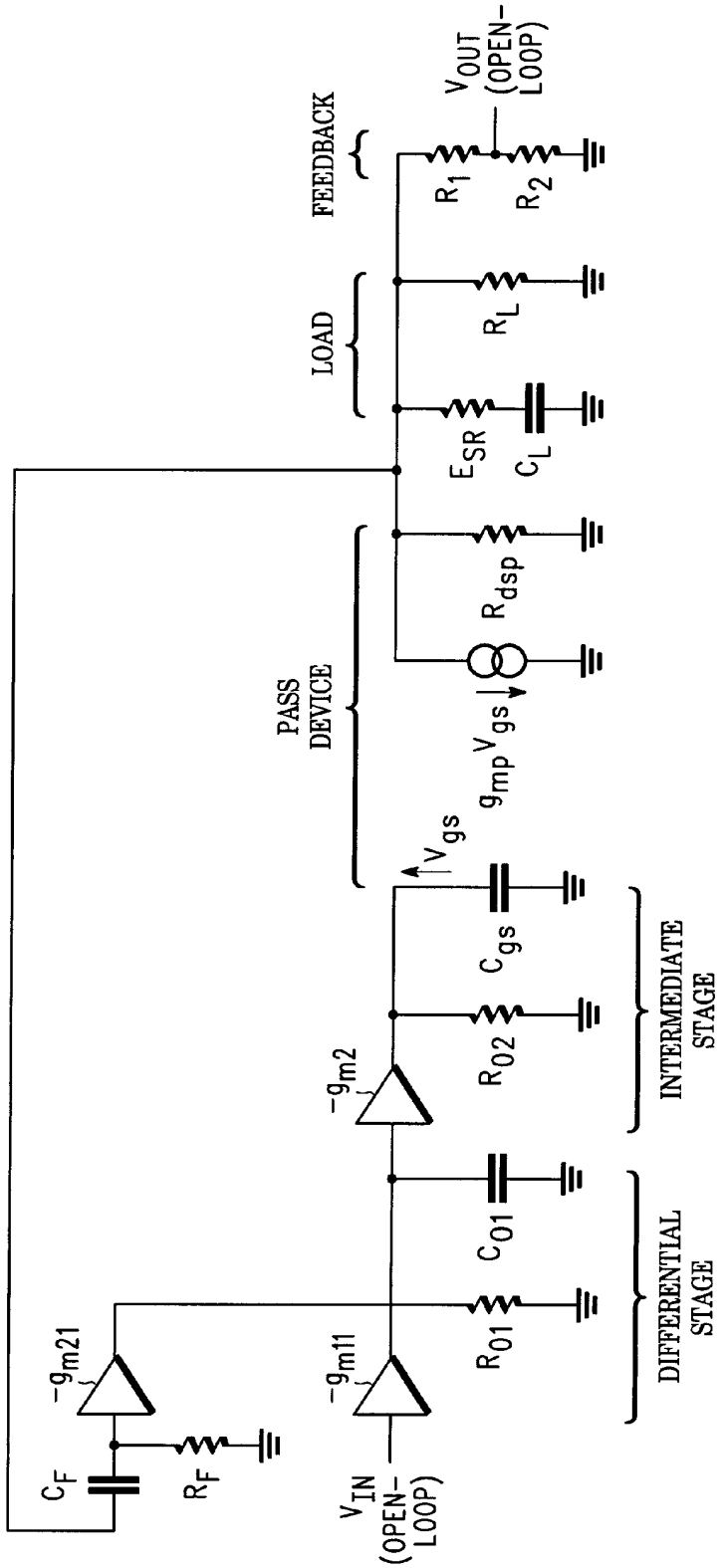

LDO
CIRCUITRY
V_O
R_L
E_{SR}
C_L
M_P
R_1
R_2
M6
M5
M51
C_F
V_{REF}
R_F
V_I
M2B
M22
GND
M4
M12
M1B
M11
M21
M3
M11
I_{BIAS}
V_{REF}

FIG. 5

FIG. 6


V_{OUT} (OPEN-LOOP)
FEEDBACK
R_1
R_2
LOAD
R_L
E_{SR}
C_L
PASS DEVICE
R_{dsp}
$g_{mp}V_{gs}$
V_{gs}
C_{gs}
INTERMEDIATE STAGE
$-g_{m2}$
R_{02}
C_{01}
DIFFERENTIAL STAGE
R_{01}
$-g_{m21}$
$-g_{m11}$
C_F
R_F
V_{IN} (OPEN-LOOP)

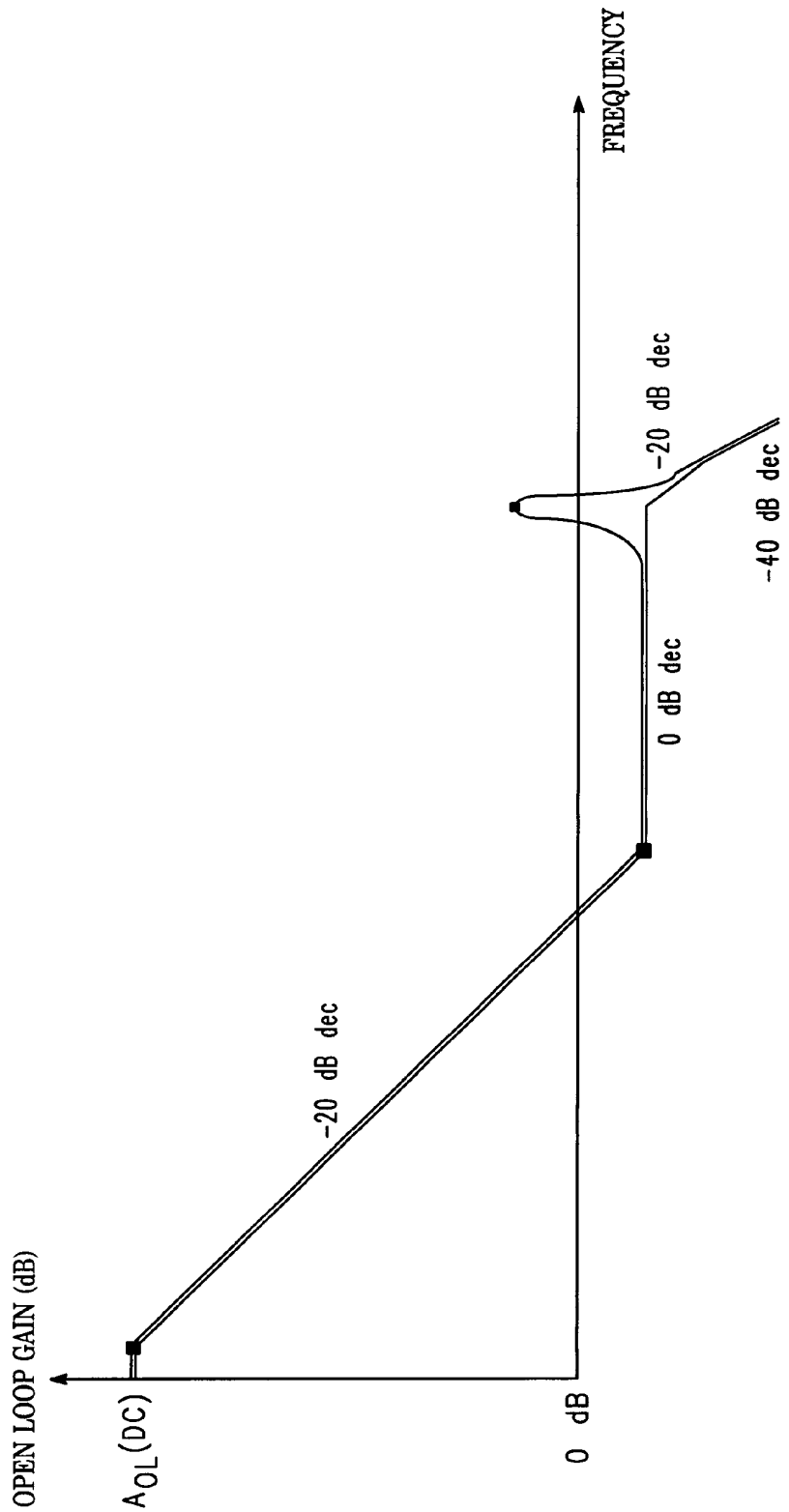

OPEN LOOP GAIN (dB)
A_{OL}(DC)
0 dB
FREQUENCY
-20 dB dec
0 dB dec
-20 dB dec
-40 dB dec

FIG. 7

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 29 0381

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 2002/005711 A1 (BAKKER ET AL) 17 January 2002 (2002-01-17) * the whole document *	1-6	G05F1/575
X	US 5 631 598 A (MIRANDA EVALDO M ET AL) 20 May 1997 (1997-05-20) * the whole document *	1-6	
X A	US 6 246 221 B1 (XI XIAOYU) 12 June 2001 (2001-06-12) * the whole document *	1,2 3-6	
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X A	EP 0 957 421 A (TEXAS INSTRUMENTS INC) 17 November 1999 (1999-11-17) * the whole document *	1,2 3-6	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7) G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 August 2002	Schobert, D

CATEGORY OF CITED DOCUMENTS

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27-08-2002

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